REMARKS

Claims 1 through 22 are pending in this case. The present Amendment amends the Specification, and it also amends independent claims 1, 8, and 16 and dependent claims 6 and 11. Reconsideration and favorable action in the above-referenced application, based on the present amendments thereto and the following remarks, are respectfully requested.

Amendments to the Specification

The present Amendment makes two grammar changes to page 11, line 7.

Rejections Under 35 U.S.C. § 112, second paragraph

Claim 6 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Specifically, the Examiner objects to the terms "high density ball grid array." In response, this Amendment deletes the quoted language from claim 6. In addition, while the Examiner did not cite claims 11 and 18 in the rejections under 35 U.S.C. § 112, second paragraph, these claims also included this language. Accordingly, this Amendment deletes the same language in claims 11 and 18.

Rejections Under 35 U.S.C. § 103(a)

Claims 1 through 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamaguchi (US Patent 5,886,876) and Ellerson et al (US Patent 5,669,137).

With respect to independent claims 1 and 8, the Examiner finds that Yamaguchi (US Patent 5,886,876) discloses all of the limitations other than potting material, and the Examiner then combines Ellerson et al (US Patent 5,669,137) with Yamaguchi (US Patent 5,886,876) to conclude that claims 1 and 8 are obvious. Applicants contend there is no suggestion to combine these references, but notwithstanding that argument Applicants note that Yamaguchi (US Patent 5,886,876) does not disclose each element cited by the Examiner, as detailed below.

Accordingly, even if these two references were combined, the result would not be as recited in claims 1 and 8.

Turning specifically to the shortcoming of Yamaguchi (US Patent 5,886,876) relative to claims 1 and 8, note that claim 1 formerly recited:

> a plurality of electrical conductors ***coupled to said chip*** and located such that each electrical conductor in said plurality of electrical conductors is aligned within a respective one of said plurality of peripheral openings in said substrate

As detailed below, Applicants respectfully submit that Yamaguchi (US Patent 5,886,876) does not show such electrical conductors, as the conductors ***coupled to*** the chip in Yamaguchi (US Patent 5,886,876) do not align as recited in claim 1. Claim 8 formerly recited other language directed to this aspect, namely:

> a chip ***having*** a plurality of bonding pads located such that each bonding pad in said plurality of bonding pads is aligned within a respective one of said plurality of peripheral openings in said substrate.

Thus, claim 8 states that the recited chip is the device ***having*** the plurality of bonding pads.

Applicants respectfully submit that claims 1 and 8, with respect to the aspect highlighted above and further detailed below, and in their form prior to this Amendment, distinguished from Yamaguchi (US Patent 5,886,876). Without prejudice and without narrowing these claims, however, Applicants attempt with this Amendment to reiterate this aspect using alternative language with the hope that such language brings this issue to the attention of the Examiner. Specifically, the above-recited language from claim 1 is amended herein with replacement terms to recite:

> a plurality of electrical conductors <u>physically attached</u> to said chip and located such that each electrical conductor in said plurality of electrical conductors is aligned within a respective one of said plurality of peripheral openings in said substrate

Similarly, the above-recited language from claim 8 is amended herein with replacement terms to recite:

> a chip having a plurality of bonding pads physically attached to the chip and located such that each bonding pad in said plurality of bonding pads is aligned within a respective one of said plurality of peripheral openings in said substrate

As detailed below, the relationship shown in these amendments, and indeed as also recited in these claims prior to the present amendment, is not shown in Yamaguchi (US Patent 5,886,876).

Turning to Yamaguchi (US Patent 5,886,876), the Examiner is correct in stating that it shows an insulating board 11 (i.e., a substrate) having a plurality of peripheral openings 19, and the patent also illustrates a chip 13 adhered to one surface of the insulating board 11. Importantly, however, note that the only conductors that could be called "coupled to" chip 13 as in the case of previous claim 1, or for which it could be said that chip 13 is "having" these conductors as in the case of previous claim 8, are the electrode pads 13a identified in the patent (see, e.g., Figure 2(a)). For example, in column 3, line 3, the patent states that these "electrode pads 13a [are] on the semiconductor device 13." Similarly, in column 4, lines 32-33, the patent states "the electrode pads 13a being upward, as shown in Figure. 2(a)." Comparably, the present Amendment recites that its "plurality of electrical conductors [are] physically attached to said chip" in claim 1, and it recites "a chip having a plurality of bonding pads physically attached to the chip" in claim 8.

Having identified the electrode pads 13a of Yamaguchi (US Patent 5,886,876), note now that such pads do not have the spatial relationship as set forth in claims 1 and 8. Specifically, claim 1 recites that its plurality of electrical conductors physically attached to said chip are:

> located such that each electrical conductor in said plurality of electrical conductors ***is aligned within a respective one of said*** plurality of ***peripheral openings*** in said substrate

Similarly, claim 8 recites that its bonding pads physically attached to the chip are:

> located such that each bonding pad in said plurality of bonding pads ***is aligned within a respective one of said*** plurality of ***peripheral openings*** in said substrate;

Antecedent support for these recitations is found in the Specification in numerous locations, as is seen in one instance with reference to Figure 1. For example, page 12, line 4 states, "A printed circuit board 70 is depicted having openings 86 around the perimeter of printed circuit board 70." Thus, these openings are recited in claims 1 and 8 as "a plurality of peripheral openings." Moreover, claims 1 and 8 recite that their respective electrical conductors or bonding pads are "***aligned within a respective one of said*** plurality of ***peripheral openings***." Thus, it can be seen in Figure 1 how bonding pads 120 are ***aligned within*** the openings 86, and this relationship is also shown by way of cross-section in Figure 2. In contrast, returning to Yamaguchi (US Patent 5,886,876) and its electrode pads 13a, it can be seen that they are not ***aligned*** to any opening at all; for example, the Examiner cites slot 19 of Yamaguchi (US Patent 5,886,876) as the claimed opening of claims 1 and 8, but it is easily seen that the electrode pads 13a of Yamaguchi (US Patent 5,886,876) are not at all "aligned within" such openings. Moreover, this claimed relationship of claims 1 and 8 gives rise to the overall formation of the device as further detailed in the Specification. As a result, Yamaguchi (US Patent 5,886,876) fails to teach the recitations of claims 1 and 8. Moreover, this deficiency is not corrected by the Examiner's citation of Ellerson et al (US Patent 5,669,137).

For the preceding reasons, Applicants respectfully submit that Yamaguchi (US Patent 5,886,876), either alone or in combination with Ellerson et al. (US Patent 5,669,137), does not show, teach, or suggest the recitations in claims 1 and 8. Accordingly, claim 1 and its dependent claims 2 through 7 and 21 are in condition for allowance, and claim 8 and its dependent claims 9 through 15 are in condition for allowance.

Independent claim 16 also previously included language comparable in various respects to the previous pending claim 1, and once again to focus the Examiner's attention to the above issue claim 16 has been amended in a comparable fashion as claim 1. Specifically, claim 16 now recites:

> a chip adhered to said second surface of said substrate, said chip having an outline that is substantially the same as said outline of said substrate and having a plurality of bonding pads physically attached to the chip and located such that each bonding pad in said plurality of bonding pads is aligned within a respective one of said plurality of peripheral openings in said substrate;

Thus, for reasons comparable to those set forth above with respect to claims 1 and 8, Applicants respectfully submit that Yamaguchi (US Patent 5,886,876), either alone or in combination with Ellerson et al (US Patent 5,669,137), does not show, teach, or suggest claim 16 either prior to, or after, this amendment in combination with the remaining recitations in claim 16. Accordingly, claim 16 and its dependent claims 17 through 20 are in condition for allowance.

With respect to claim 22, the Examiner also finds that Yamaguchi (US Patent 5,886,876) discloses all of the limitations other than potting material, and the Examiner then combines Ellerson et al (US Patent 5,669,137) with Yamaguchi (US Patent 5,886,876) to conclude that claim 22 is obvious. Claim 22 is herein separately addressed because it does not recite the limitation noted above with respect to conductors or bonding pads physically attached to a chip and aligned as described above. However, claim 22 does recite the following:

> a substrate having a plurality of openings and first and second surfaces;
>
> a chip comprising an operative side and a non-operative side, wherein said chip is adhered to said second surface of said substrate such that the non-operative side faces away from the substrate; . . and
>
> potting material filing said peripheral openings.

Note that in claim 22, and in contrast to Yamaguchi (US Patent 5,886,876), there are recited the "operative side and a non-operative side" of the claim 22 chip and the directionality in that the "non-operative side faces away from the substrate." Yamaguchi (US Patent

5,886,876) does not explicitly discuss either an "operative side" or a "non-operative side" of its integrated circuit 13. However, it may be rightfully argued that its operative side is the side discussed above from which the electrode pads 13a protrude and, hence, the operative side is the upward side in Yamaguchi (US Patent 5,886,876) Figure 2(a). Indeed, this argument is further supported in that Yamaguchi (US Patent 5,886,876) later describes that it adds a sealing material 22 on top of its integrated circuit 13, and presumably this material is required to seal the operative (and upward facing) side of its integrated circuit 13. Accordingly, the Yamaguchi (US Patent 5,886,876) ***operative*** side faces away from its insulating board 11. In contrast, claim 22 recites with respect to its chip that it is the ***non-operative side*** of the chip that "faces away from the substrate." Indeed, this allows the encapsulation and sealing considerations to be different than those shown in Yamaguchi (US Patent 5,886,876). Specifically, Yamaguchi (US Patent 5,886,876) in effect encloses both the operative and non-operative side of its chip, using its insulating board to enclose the non-operative side and using sealing material 22 (Figure 2(c)) to enclose the operative side.[1] In contrast, due to the relationship of the non-operative side facing away from the substrate as recited in claim 22, then in one embodiment the following aspects may be achieved, as set forth in the Specification at page 27, lines 7-10, which state:

> The potting and encapsulation of the integrated circuit package 30 of the present invention as described herein also reduces the overall profile ***by allowing the non-operative or backside of the silicon chip 50 to be exposed.***

No such result of exposure is shown in Yamaguchi (US Patent 5,886,876), where, instead, that patent teaches fully enclosing its integrated circuit because the operative side of its integrated circuit faces away from its insulating board. Accordingly, and in view of the above, Applicants respectfully submit that that Yamaguchi (US Patent 5,886,876), either alone or in combination with Ellerson et al (US Patent 5,669,137), does not show, teach, or suggest claim 22.

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[1] In an alternative embodiment, Yamaguchi (US Patent 5,886,876) uses a metallic cover 25 (Figure 6) to seal the operative side of its integrated circuit.

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Fees

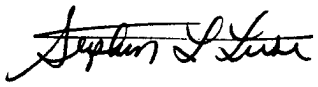
The fee for the enclosed petition for an extension of time for a two (2) month extension is addressed in the Fee Transmittal (for FY 2001) sheet filed herewith.

The Commissioner is also hereby requested and authorized to charge any additional fees necessary for the filing of the enclosed papers to deposit account number 20-0668 of Texas Instruments Incorporated.

Conclusion

From the above, Applicants respectfully submit that all of the pending claims in this case are patentably distinct in view of the record in this case. Entry of the above amendment in, and reconsideration of, the above-referenced application are respectfully requested.

Respectfully submitted,



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August 21, 2001

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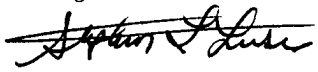

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Version with markings to show changes made:

In the Specification:

For the paragraph on page 11, lines 1 through 13:

As defined herein, the term "profile" refers to thickness or height of, for example, the integrated circuit package of the present invention. The integrated circuit package of the present invention may be measured in, for example, mils. As defined herein, the term "substantially similar" refers to the relative outlines of the printed circuit board and the silicon chip, which are within less than about 10% of one another [other]. In one embodiment of the present invention, the difference in the outlines is about 2%. In an alternative embodiment, the silicon chip and the printed circuit board have the same outlines. Importantly, the term substantially similar does not indicate which of the two components is larger, as either form is encompassed by the present invention.

In the claims:

1 (twice amended). An integrated package comprising:

a substrate having a plurality of peripheral openings and first and second surfaces;

a chip adhered to said second surface of said substrate;

a plurality of electrical conductors physically attached [coupled] to said chip and located such that each electrical conductor in said plurality of electrical conductors is aligned within a respective one of said plurality of peripheral openings in said substrate;

a plurality of pads disposed on said first surface of said substrate generally centralized within said peripheral openings of said substrate; and

potting material filling said peripheral openings.

6 (amended). The integrated circuit package as recited in claim 1 further comprising a plurality of solder balls disposed on said pads [forming a high density ball grid array].

8 (twice amended). An integrated circuit package comprising:

a substrate having a plurality of peripheral openings and first and second surfaces;

a plurality of routing strips being integral with said substrate;

a plurality of pads disposed centrally on said first surface, at least one of said pads being electrically connected with at least one of said routing strips;

potting material filling said plurality of peripheral openings;

a chip having a plurality of bonding pads physically attached to the chip and located such that each bonding pad in said plurality of bonding pads is aligned within a respective one of said plurality of peripheral openings in said substrate; and

wire bonding electrically connecting said chip to said substrate between said bonding pads and said routing strips.

11 (amended). The integrated circuit package as recited in claim 8 further comprising a plurality of solder balls disposed on said pads [forming a high density ball grid array].

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16 (twice amended). An integrated circuit package comprising:

a substrate having a plurality of peripheral openings, first and second surfaces and an outline;

a plurality of routing strips being integral with said substrate;

a plurality of pads centrally disposed on said first surface at least one of said pads being electrically connected with said routing strips;

a chip adhered to said second surface of said substrate, said chip having an outline that is substantially the same as said outline of said substrate and having a plurality of bonding pads physically attached to the chip and located such that each bonding pad in said plurality of bonding pads is aligned within a respective one of said plurality of peripheral openings in said substrate;

wire bonding electrically connecting said bonding pads to said routing strips;

vias connecting said routing strips to said pads;

potting material filling said peripheral openings and covering said wire bonding and said bonding pads; and

a plurality of solder balls centrally disposed on said pads disposed on said first surface of said substrate [forming a high density ball grid array].